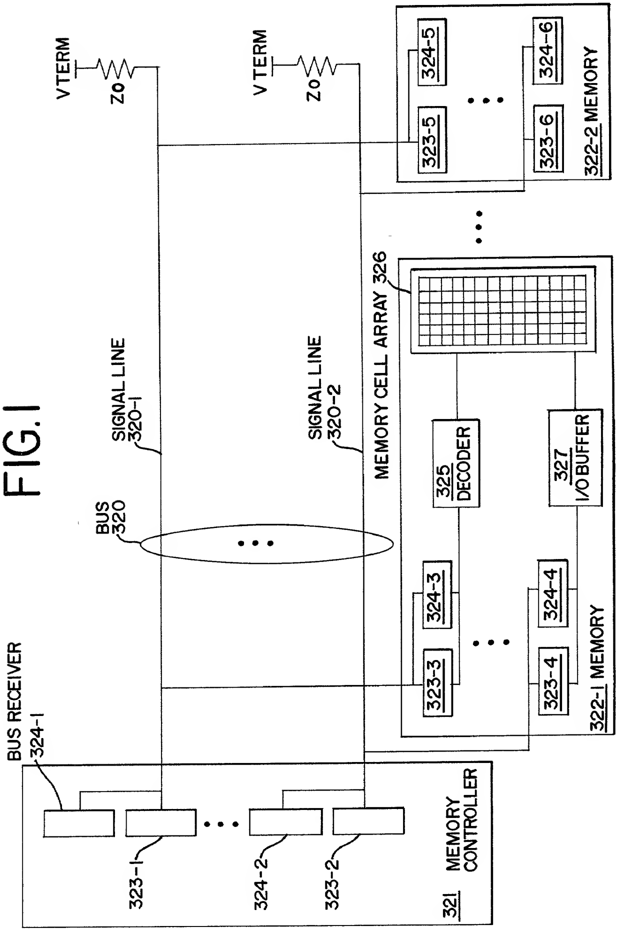

VTERM
Zo
V TERM
Zo
323-5
324-5
323-6
324-6
322-2 MEMORY
SIGNAL LINE
320-1
SIGNAL LINE
320-2
MEMORY CELL ARRAY 326
325
DECODER
327
I/O BUFFER
BUS
320
BUS RECEIVER
324-1
323-3
324-3
323-4
324-4
322-1 MEMORY
323-1
324-2
323-2
321
MEMORY
CONTROLLER

FIG. 1

FIG.2

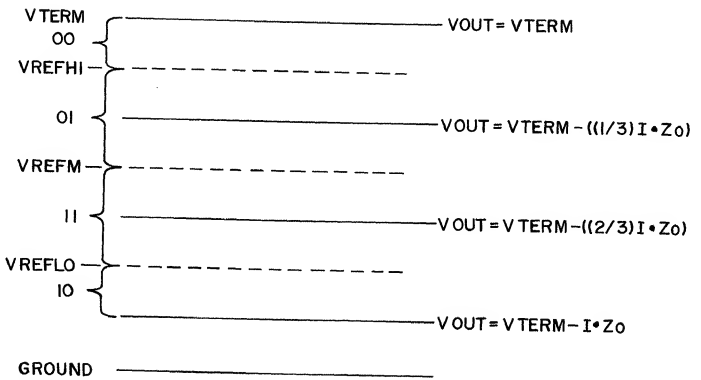


FIG.3A

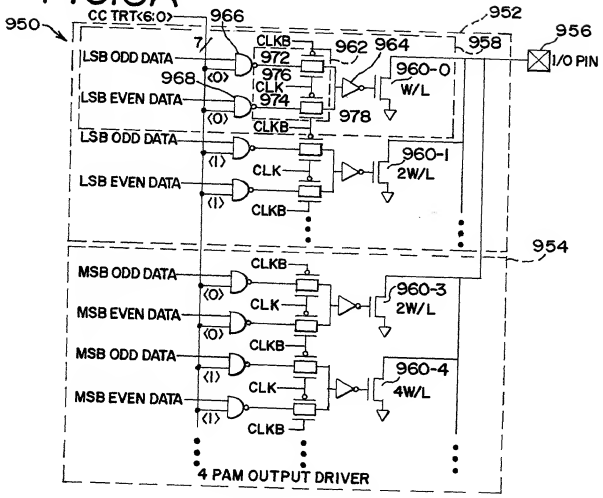


FIG.3B

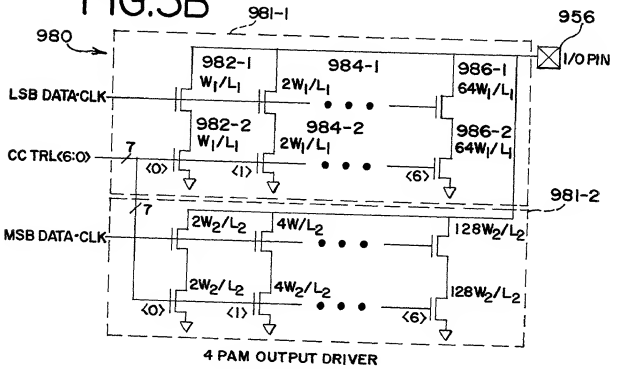


FIG. 4A

FIG. 4B

FIG. 4C

FIG.5A

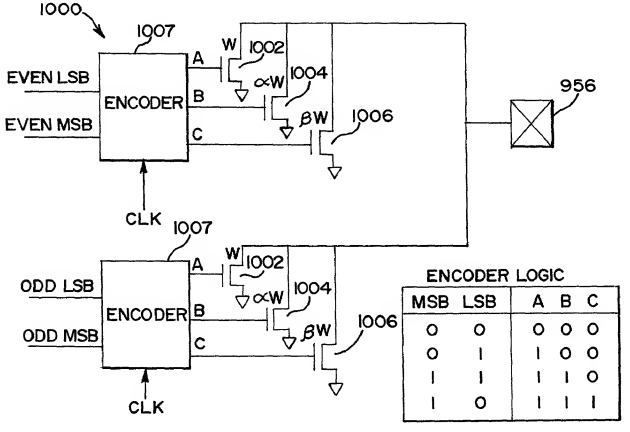


FIG.5B

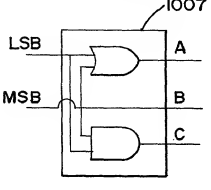


FIG.5C

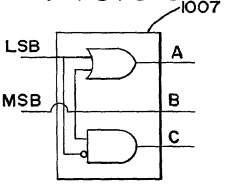
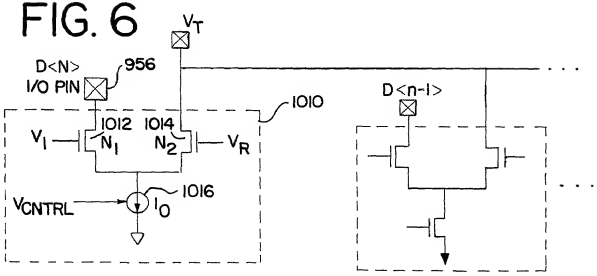


FIG. 6



CIRCUIT TO REDUCE SWITCHING NOISE

FIG. 7

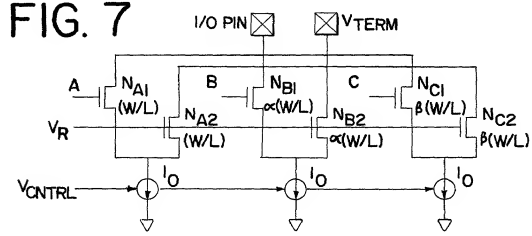
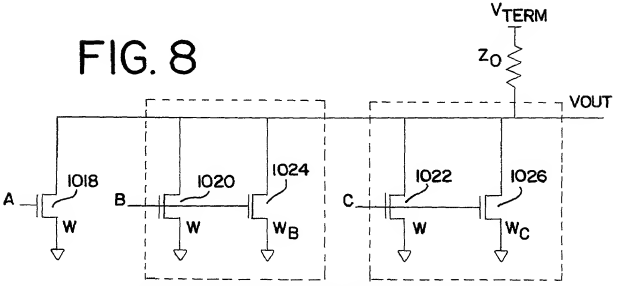
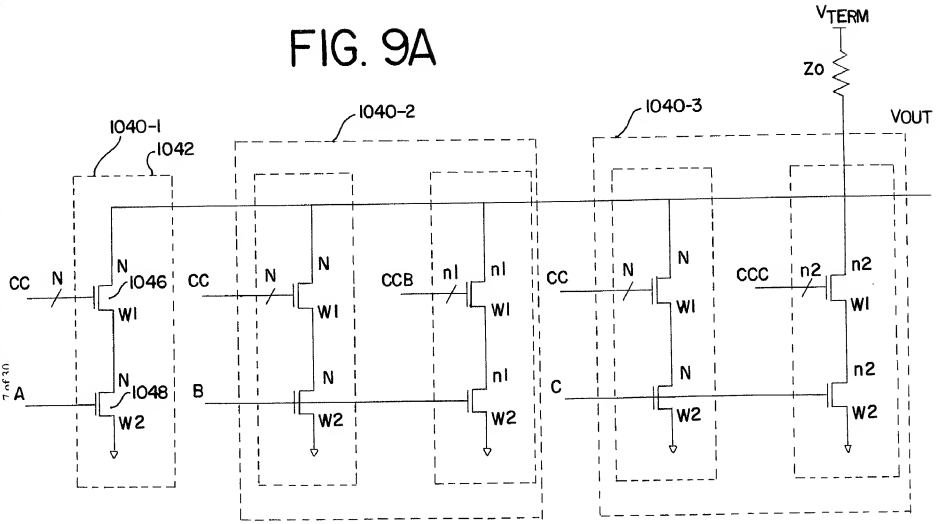


FIG. 8



GDS COMPENSATED MULTI-PAM OUTPUT DRIVER

FIG. 9A



GDS COMPENSATED MULTI-PAM OUTPUT DRIVER WITH CURRENT CONTROL

FIG. 9B

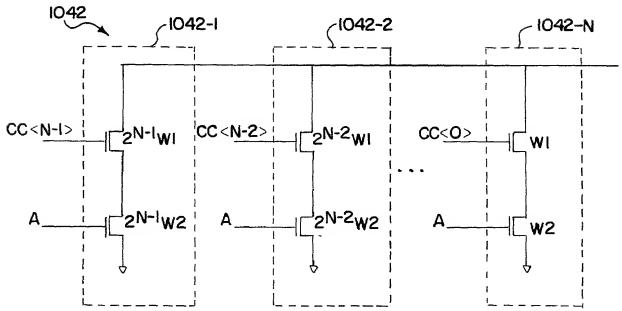


FIG. 9C

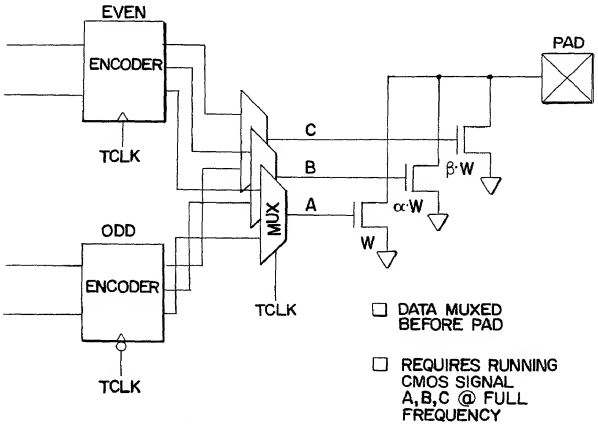
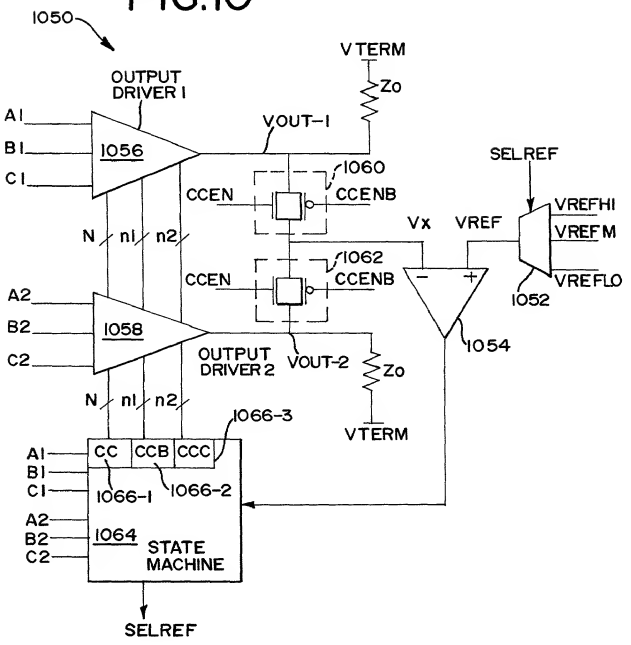
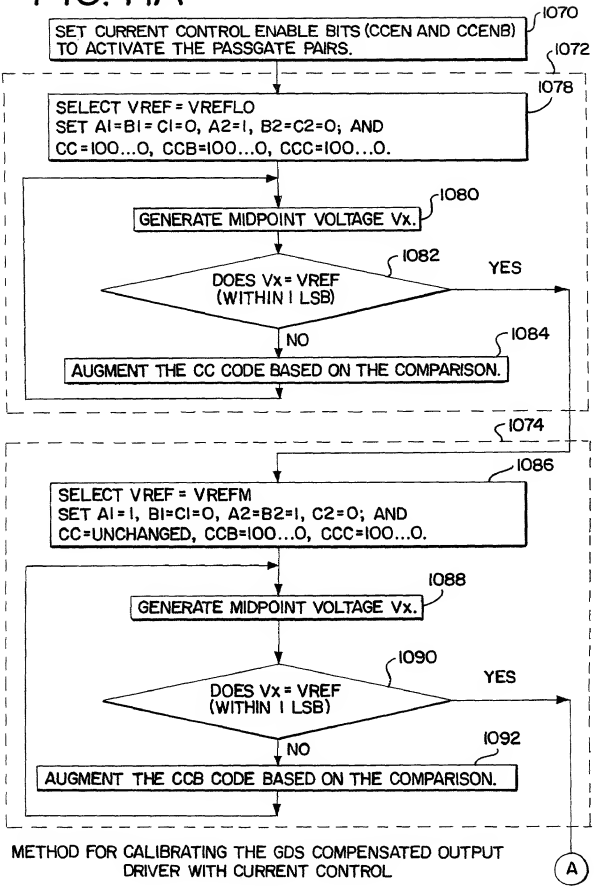


FIG.10



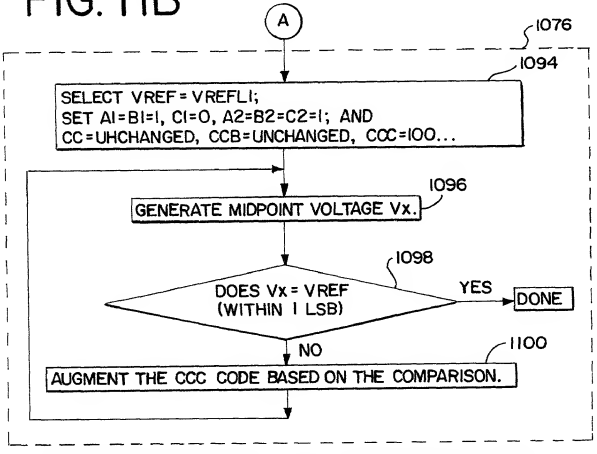
CIRCUIT FOR CALIBRATING THE GDS COMPENSATED OUTPUT DRIVER WITH CURRENT CONTROL

FIG. 11A



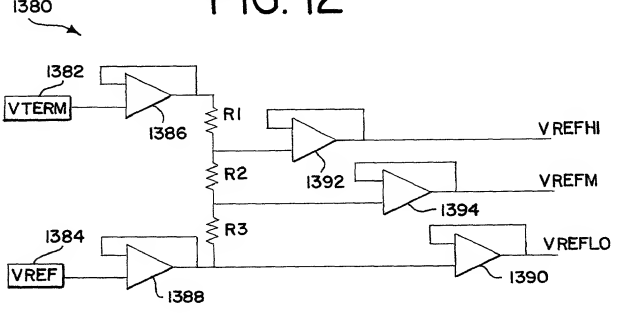
METHOD FOR CALIBRATING THE GDS COMPENSATED OUTPUT DRIVER WITH CURRENT CONTROL

FIG. 11B



METHOD FOR CALIBRATING THE GDS COMPENSATED OUTPUT DRIVER WITH CURRENT CONTROL

FIG. 12



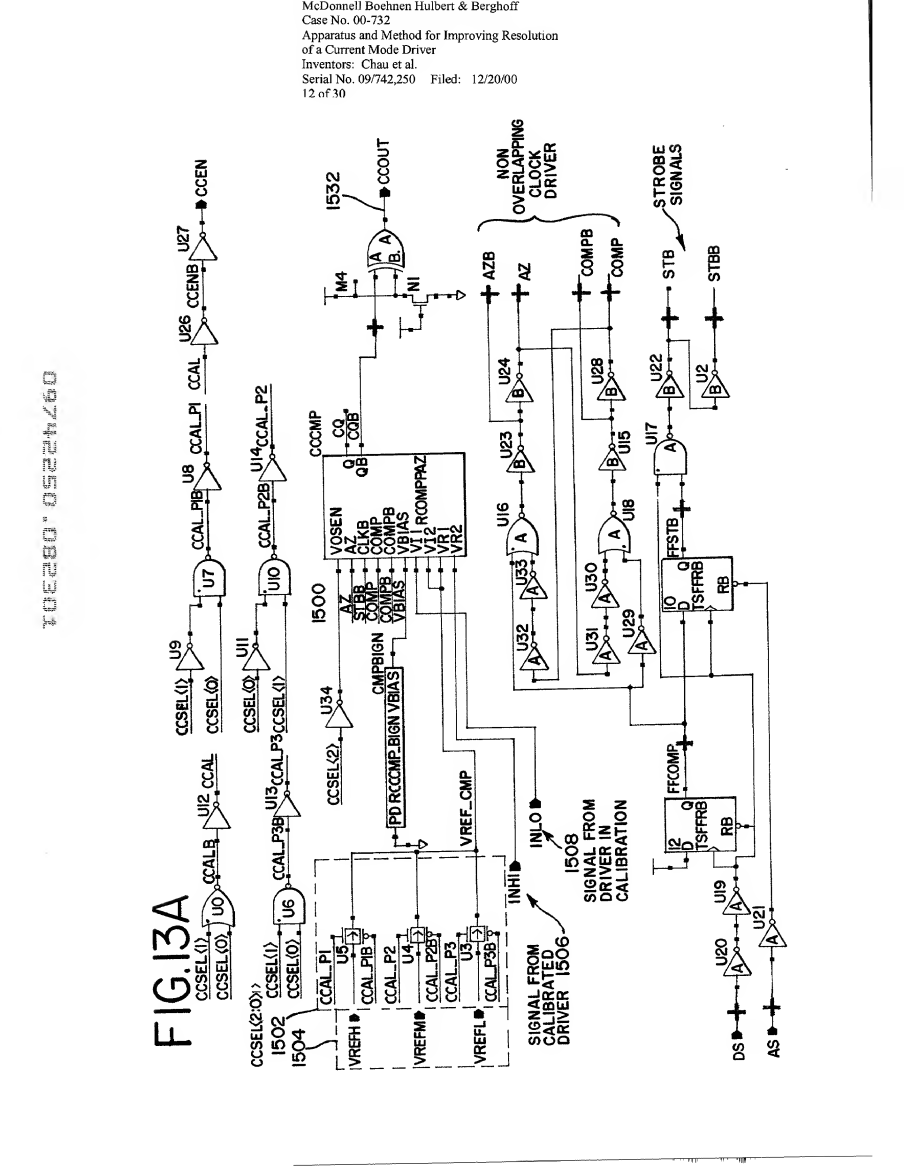


FIG.13A

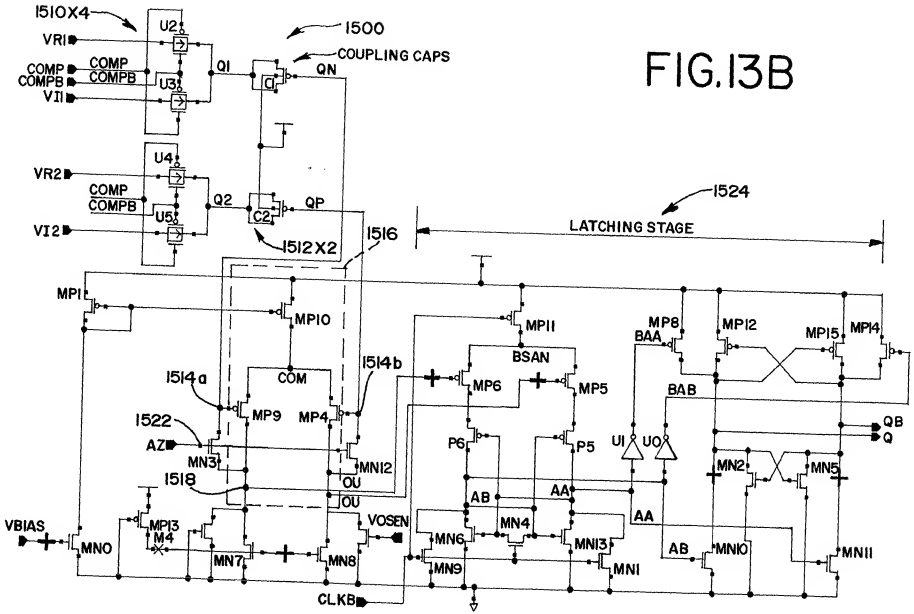


FIG.13B

FIG.13C

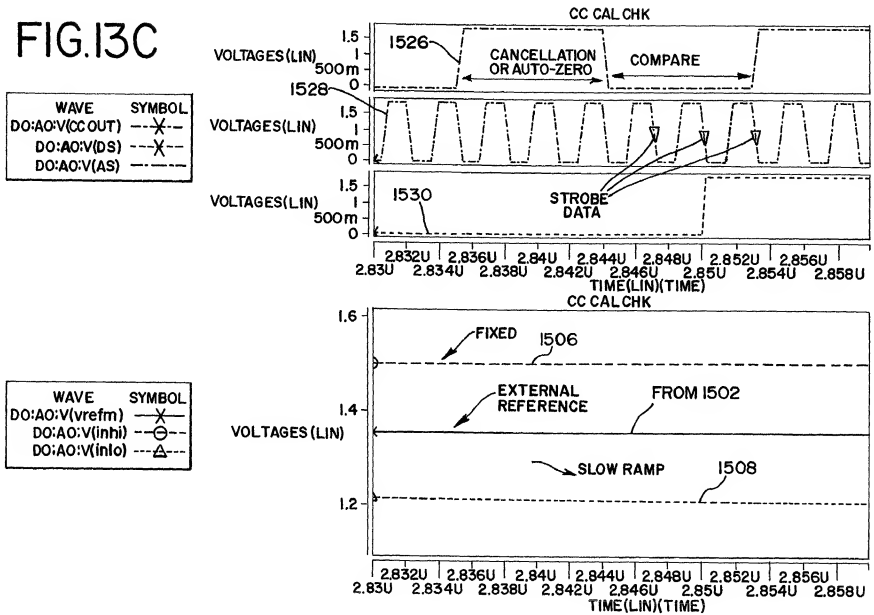


FIG. 13D

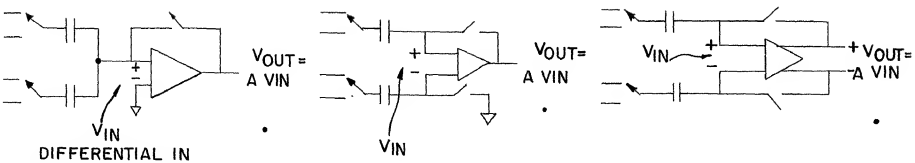
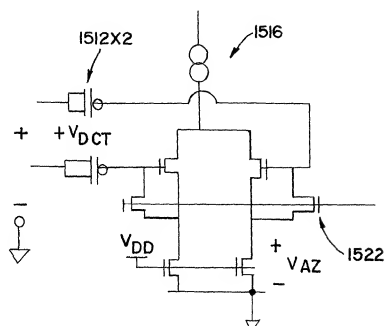
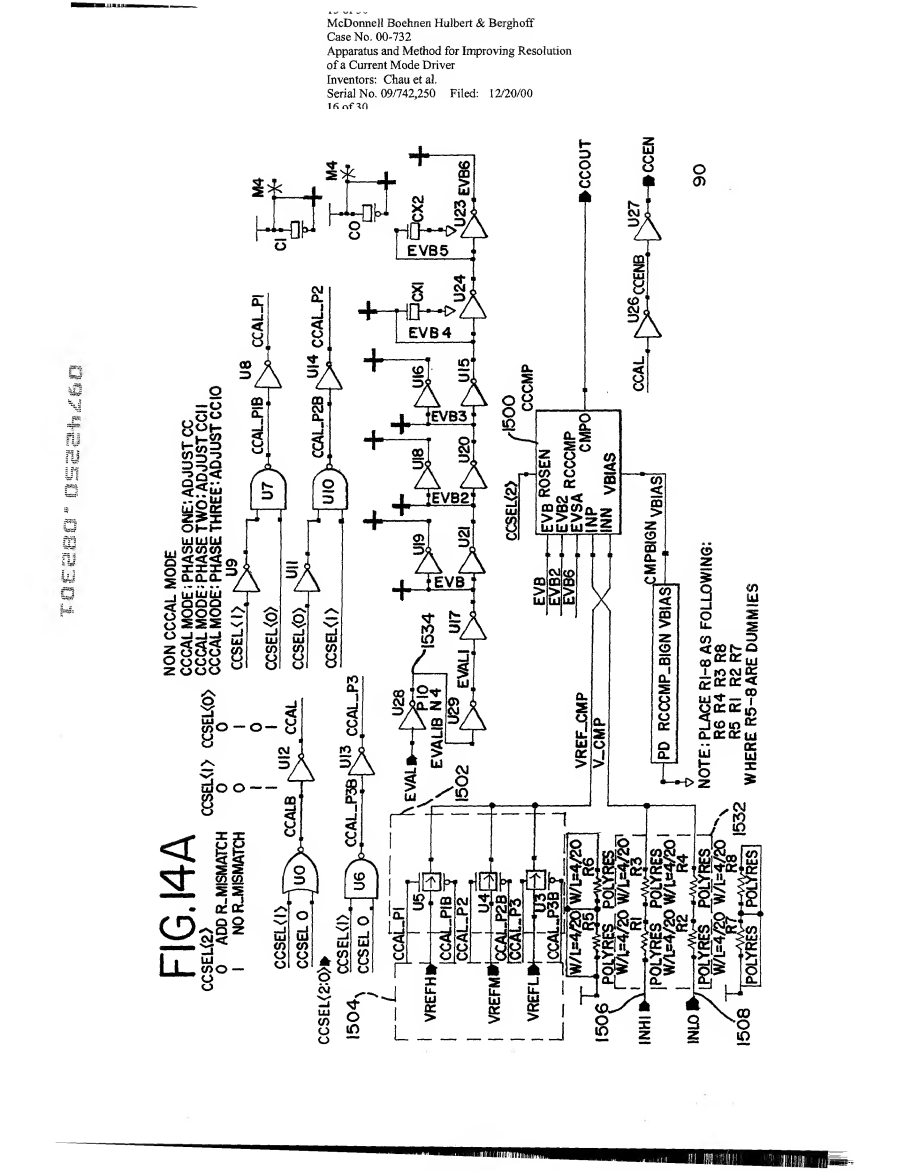


FIG. 13E





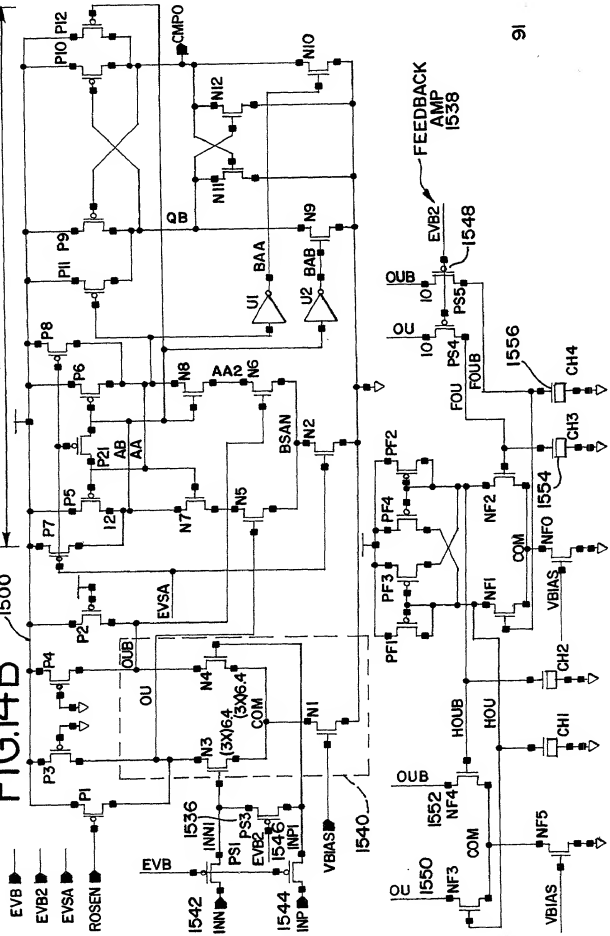


FIG.14C

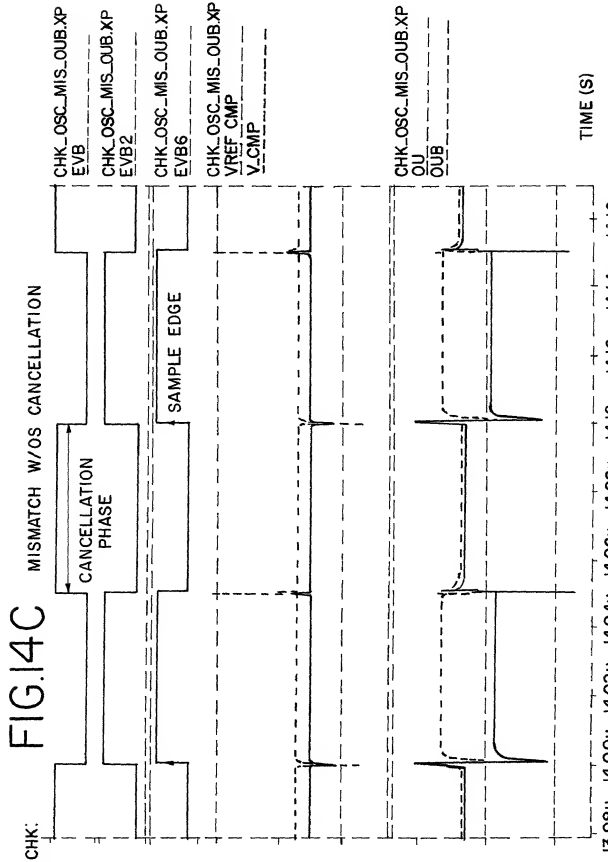


FIG.14D

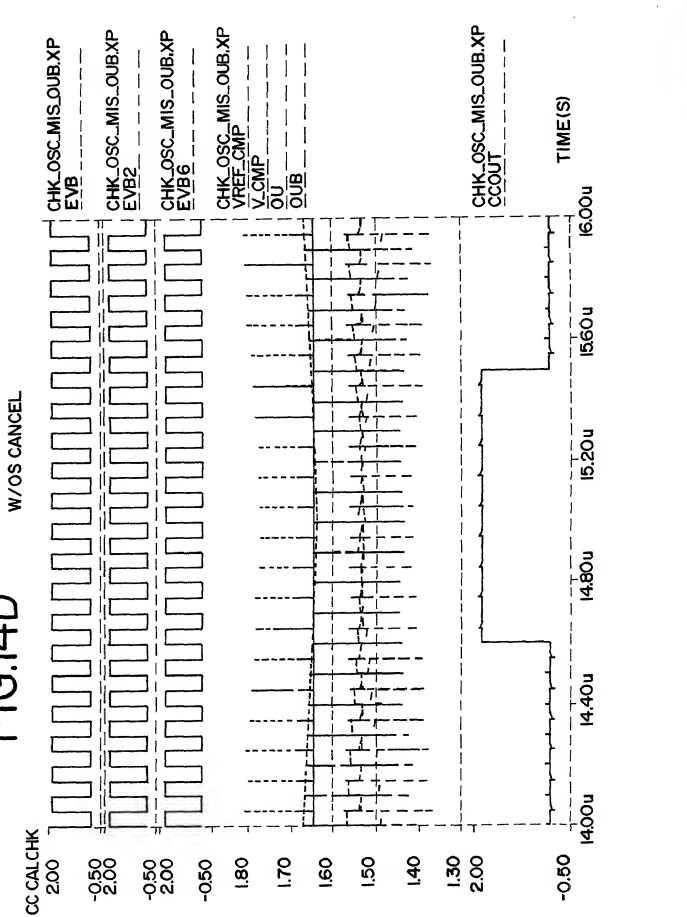


FIG.15A

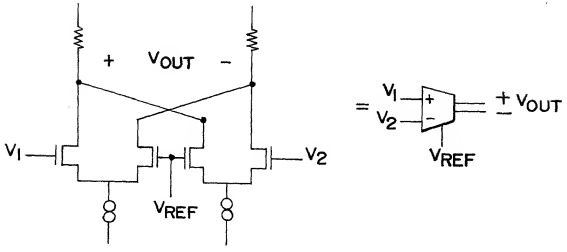


FIG.15B

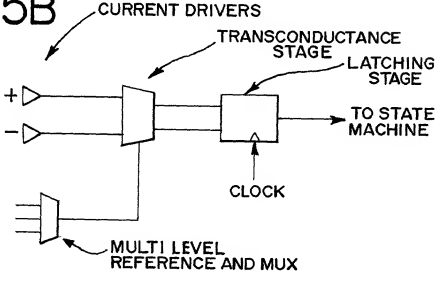


FIG.16

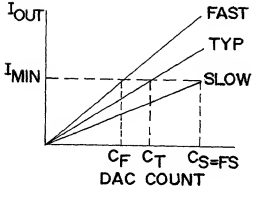
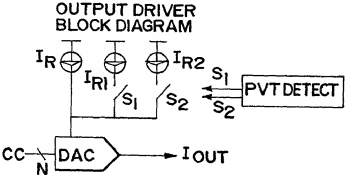


FIG.17



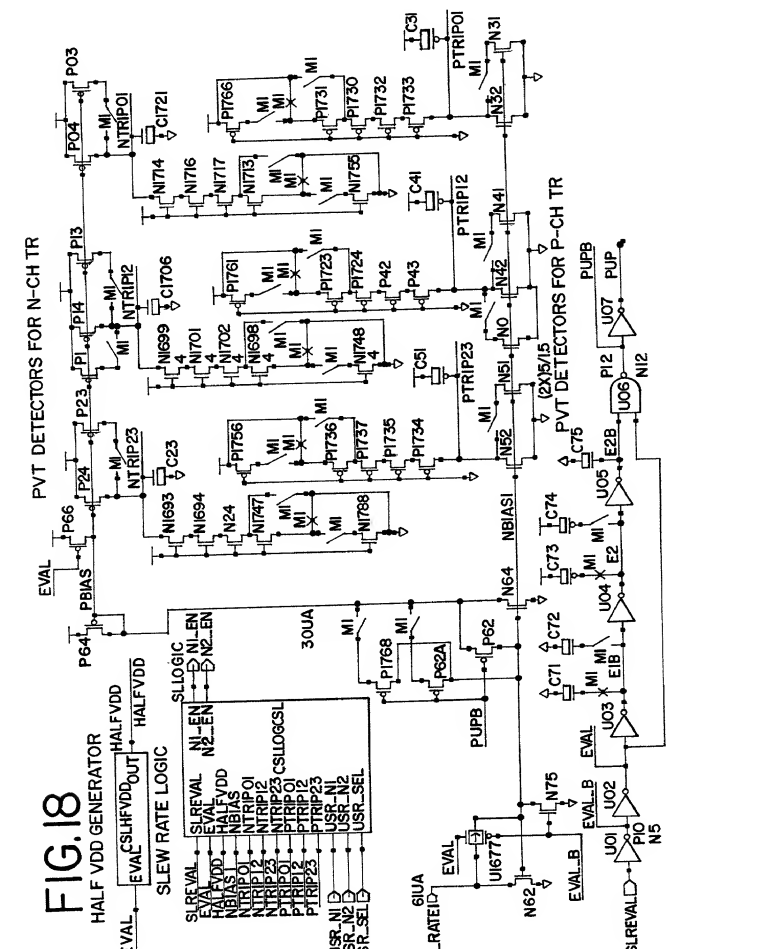


FIG. 18

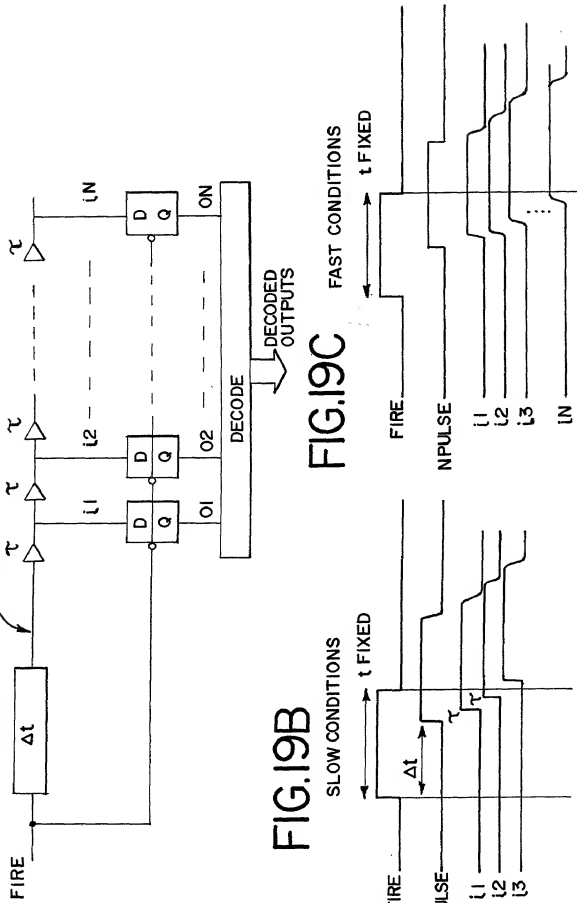


FIG.19A

FIG.19B

FIG.19C

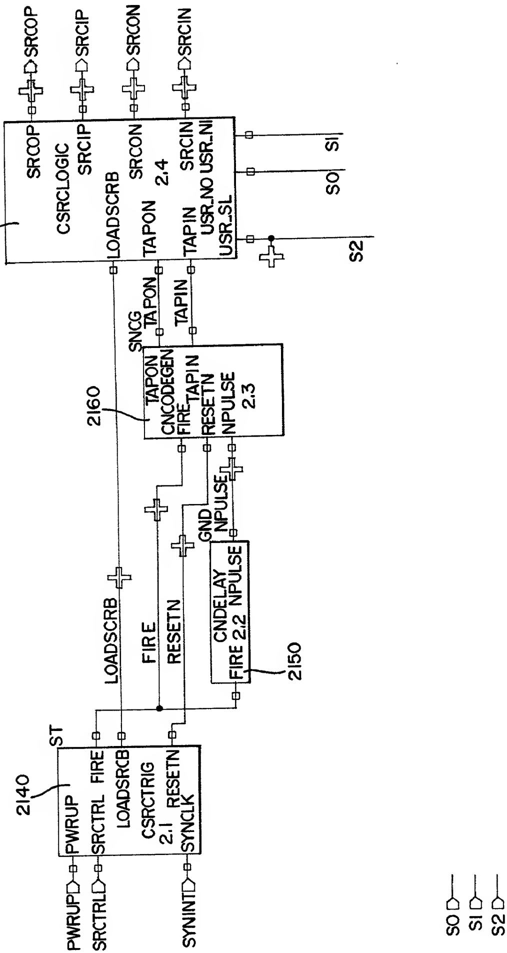

SRCOP
SRCIP
SRCON
SRCIN
SL
2170
SRCOP
CSRCLOGIC
SRCIP
LOADSCRB
SRCON
2.4
TAPON
SRCIN
TAPIN
USR_NO USR_NI
USR_SL
SI
SO
S2
SNCG
TAPON
TAPIN
2160
TAPON
CNCODEGEN
FIRE
TAPIN
RESETN
NPULSE
2.3
GND
NPULSE
LOADSCRB
FIRE
RESETN
CNDELAY
FIRE 2.2 NPULSE
2150
2140
ST
PWRUP
SRCTRL FIRE
LOADSRCB
CSRCTRIG
2.1 RESETN
SYNCLK
PWRUP
SRCTRL
SYNINT
SO
SI
S2

FIG.20A

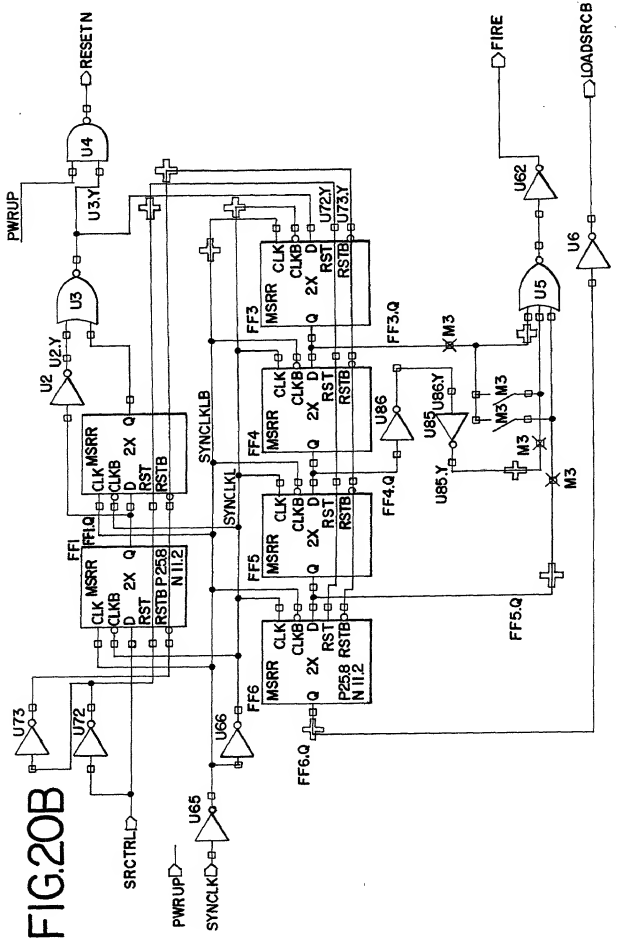


FIG.20B

FIG.20C

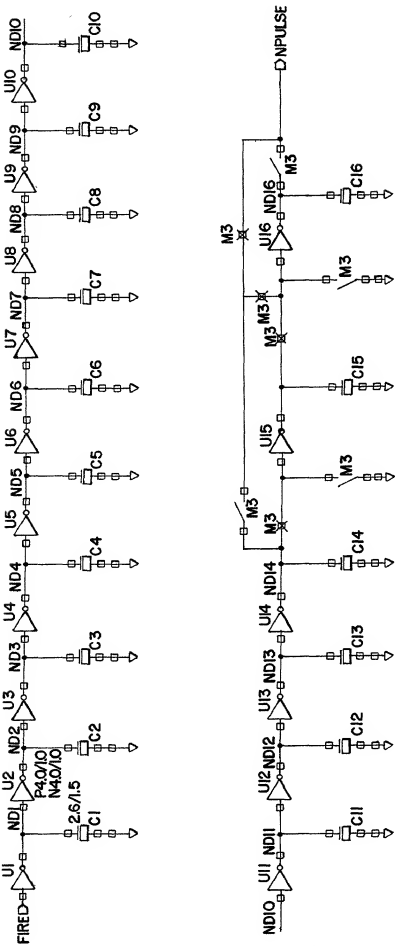


FIG.20D

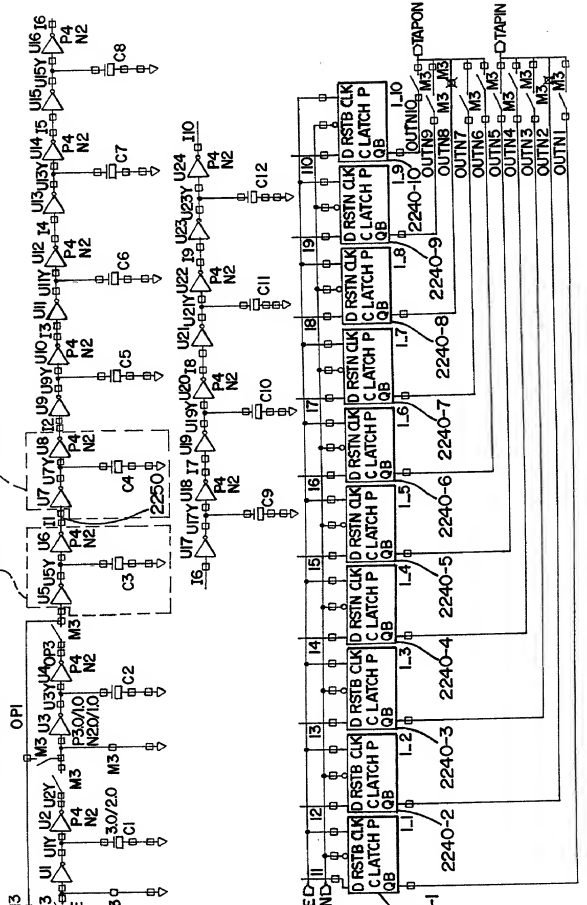


FIG.20E

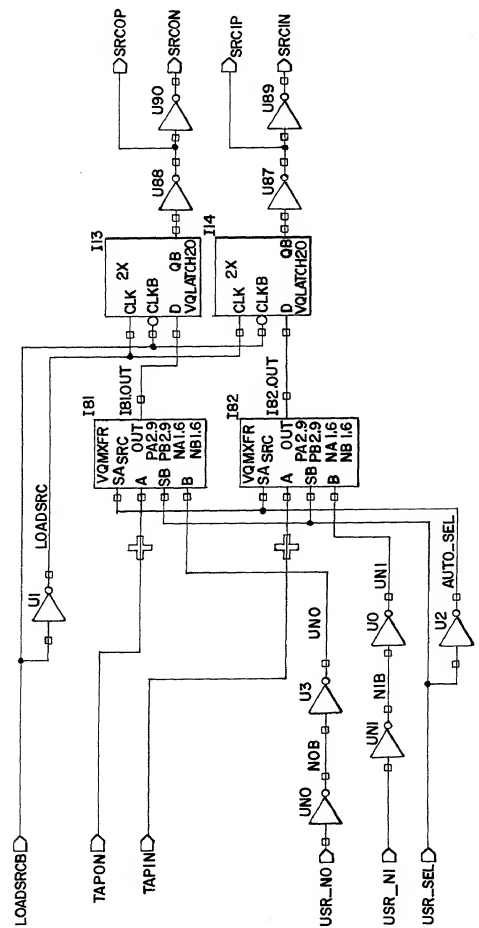


FIG.21A

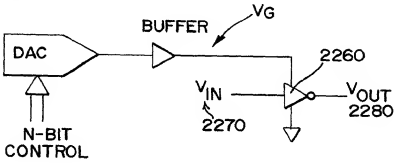


FIG.21B

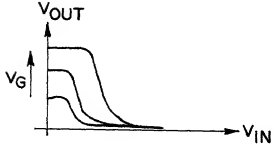


FIG.22

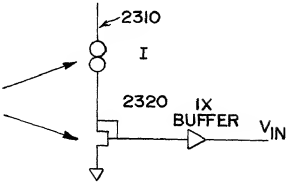


FIG.23

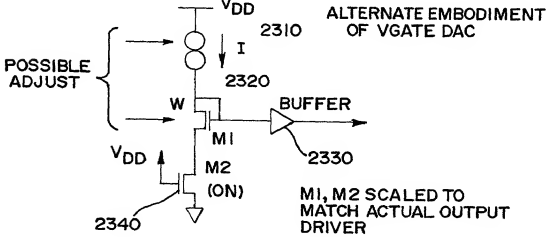


FIG.24A

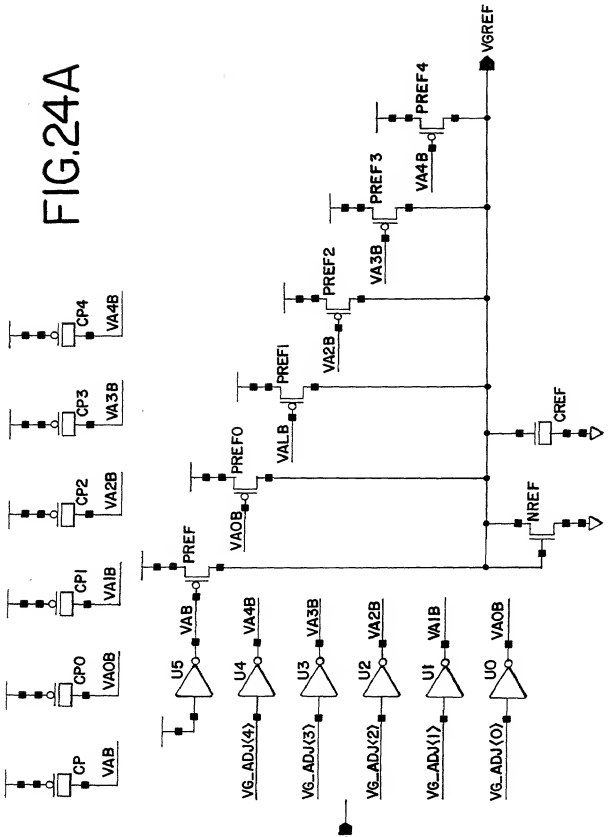


FIG.24B